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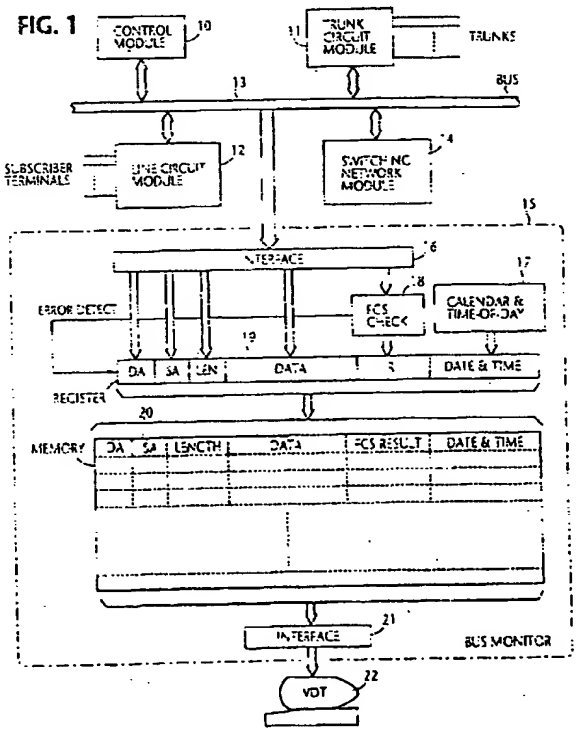
(54) Bus monitor circuit for switching system and method of monitoring.

(57) In a switching system, a data bus which interconnects circuit modules, a switching network module and a control module for transporting packets between the interconnected modules. A bus interface (16) is connected to the data bus (13) for receiving a copy of every packet on the data bus. An error detector (18) determines whether the received packet contains an error, and produces an error detect signal and an error check result if the received packet is determined as having an error. In response to the error detect signal, the received packet, the error check result and time-of-day data are stored into a register (19) and transferred to one of the storage locations of a memory (20) to keep a list of error records. A maintenance station (22) reads stored error records from the memory for identifying the source of errors.

FIG. 1



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The present invention relates generally to a bus monitor circuit for a switching system, and to a method of monitoring a packet on the data bus of a switching system. The invention also relates to a switching system including the bus monitor circuit, and more specifically to a maintenance system for keeping error records of a switching system.

In conventional switching systems, functional modules are interconnected by a data bus and packets are transported between the modules over the data bus. When an abnormal condition occurs in the system, a logic analyzer is brought into the system and hand-wired to the data bus for monitoring the packets transported along the bus. However, the use of the logic analyzer requires a special team of experts. Additionally, the logic analyzer is not provided with a sufficient amount of memory for storing records to be analyzed to allow identification of the fault.

The present invention therefore seeks to provide a bus monitor circuit for monitoring packets on the data bus of a switching system and keeping error records for maintenance purposes.

According to the present invention, there is provided a bus monitor circuit for a switching system. The switching system comprises circuit modules, a switching network module, and a control module for controlling the circuit modules and the switching module. All the modules are interconnected by a data bus for transporting a packet between the interconnected modules. The bus monitor circuit comprises a memory having a plurality of storage locations, time-keeping means for generating time-of-day data, and an interface connected to the data bus for receiving a copy of the packet therefrom. An error detector is provided for determining whether the packet contains an error, and producing an error detect signal and an error check result if the packet is determined as having an error. In response to the error detect signal, the copy of the packet, the error check result and the time-of-day data are stored into one of the storage locations of the memory. A maintenance station is provided for reading stored contents of the memory.

The present invention will be described in further detail, by way of example,with reference to the accompanying drawings, in which:

Fig. 1 shows in block form a switching system embodying a bus monitor of the present invention; and

Fig. 2 shows the structure of signals transported on the data bus of Fig. 1.

Referring now to Fig. 1, there is shown a switching system according to a preferred embodiment of the present invention. The switching system, inter-office trunks or transmission lines are terminated at a trunk circuit module 11 which controls the inter-office trunks in response to a command signal from a control module 10. Subscriber lines are terminated at a line circuit module 12 which controls the subscriber lines in response to a command signal from the control module 10. Both of circuit modules 11 and 12 are connected to a data bus 13 to transfer data and speech signals to a switching network module 14 where these signals are switched between lines and trunks by way of the data bus under control of the control module 10 in a manner known in the art. The control module 10 further provides an overall control of the system including maintenance and administrative tasks of the system. As shown in Fig. 2, the signal transported on the data bus 13 comprises a data signal 30 and a delimiter 31 which indicates the effective area of the data signal. The data signal is transmitted in packet format which begins with a destination address field (DA) followed by a source address field (SA), a data length field (LEN), a data field (DATA) and a frame check sequence field (FCS) for detecting error bits.

According to the preferred embodiment of the present invention, a bus monitor 15 is provided which comprises a bus interface 16 connected to the data bus 13 for receiving every packet transported on the data bus using a delimiter 31 as a gate pulse and supplying the DA, SA, LEN and DATA fields of a copy of the received packet to a register 19 and the FCS field of the packet to a known FCS check circuit 18 as illustrated. A calendar and time-of-day clock source 17 is provided for generating date and time-of-day data. If an error is detected as a result of an FCS check, the FCS check circuit 18 produces an error detect signal and applies it to the register 19 as an enable pulse to store the DA, SA, LEN and DATA fields of the copy of the packet to corresponding storage areas of register 19 and the result of the FCS check into a result area "R" of the register. At the same time, the date and time-of-day data are supplied to a "DATE & TIME" area of the register.

When register 19 is filled, all the stored error-containing data are transferred from the register to a memory 20 as a first error record. When a subsequent packet is received from the data bus, a similar process is repeated and stored into the memory 20 with an FCS check result and date and time-of-day data as a second error record if the subsequent packet is determined as containing an error. If no error is detected by the FCS check circuit 18, no record is stored in memory 20. As the process continues, the memory 20 will be filled with a plurality of error records as system diagnostic data.

At an appropriate time, all the stored error records are read from the memory 20 by way of an interface 21 into a maintenance station or video display terminal 22 to provide a display of a list of error records on a video screen. The displayed error records may be analyzed by maintenance personnel to locate the source of the trouble.

In summary, the preferred embodiment of

switching system according to the present invention includes a data bus which interconnects circuit modules, a switching network module and a control module for transporting packets between the interconnected modules. A bus interface is connected to the data bus for receiving a copy of every packet on the data bus. An error detector determines whether the received packet contains an error, and produces an error detect signal and an error check result if the received packet is determined as having an error. In response to the error detect signal, the received packet, the error check result and time-of-day data are stored into a register and transferred to one of the storage locations of a memory to keep a list of error records. A maintenance station reads stored error records from the memory for identifying the source of errors.

It will be understood that the present invention has been described above purely by way of example, and modifications of detail can be made within the scope of the invention.

Claims

1. A bus monitor circuit for a switching system comprising a plurality of circuit modules, a switching network module, a control module for controlling said circuit modules and said switching module, and a data bus interconnecting said circuit modules, said switching network module and said control module for transporting a packet between the interconnected modules, the bus monitor circuit comprising:

   time-keeping means for generating time-of-day data;

   means connected to said data bus for receiving a copy of the packet therefrom;

   means for determining whether the received copy of said packet contains an error, and producing an error detect signal and an error check result if the copy of the packet is determined as having an error;

   a memory having a plurality of storage locations for storing the copy of the packet, the error check result and the time-of-day data into one of the storage locations in response to said error detect signal; and

   a maintenance station for reading stored contents of said memory.

2. A bus monitor circuit as claimed in claim 1, wherein the time-keeping means further generates a calendar date signal which is stored into said storage location of the memory in response to said error detect signal.

3. A bus monitor circuit for a switching system comprising a plurality of circuit modules, a switching network module, a control module for controlling said circuit modules and said switching module, and a data bus interconnecting said circuit modules, said switching network module and said control module for transporting a packet between the interconnected modules, said packet comprising a destination address, a source address, a data field and a frame check sequence (FCS), the bus monitor circuit comprising:

   time-keeping means for generating time-of-day data;

   an interface connected to said data bus for receiving a copy of the packet therefrom;

   an FCS check means for receiving the frame check sequence of the copy of said packet and determining whether the packet contains an error, and producing an error detect signal and an error check result if said packet is determined as having an error;

   register means for storing the destination address, the source address and the data field of the copy of the packet, said error check result and the time-of-day data to produce an error record;

   a memory having a plurality of storage locations for storing said error record into one of the storage locations of said memory in response to said error detect signal; and

   a maintenance station for reading stored error records from said memory.

4. A bus monitor circuit as claimed in claim 3, wherein the time-keeping means further generates a calendar date signal which is stored into said storage location of the memory in response to said error detect signal.

5. A method of monitoring a packet on the data bus of a switching system, said switching system comprising a plurality of circuit modules, a switching network module, a control module for controlling said circuit modules and said switching module, and a data bus interconnecting said circuit modules, said switching network module and said control module for transporting a packet between the interconnected modules, the method comprising:

   generating time-of-day data;

   receiving a copy of the packet from the data bus;

   determining whether the received copy of said packet contains an error, and producing an error detect signal and an error check result if the copy of the packet is determined as having an error;

   storing in a memory the copy of the packet, the error check result and the time-of-day data in response to said error detect signal; and

reading stored contents of said memory

6. A method of monitoring a packet on the data bus of a switching system, said switching system comprising a plurality of circuit modules, a switching network module, a control module for controlling said circuit modules and said switching module, and a data bus interconnecting said circuit modules, said switching network module and said control module for transporting a packet between the interconnected modules, said packet comprising a destination address, a source address, a data field and a frame check sequence, the method comprising;

generating time-of-day data;

receiving a copy of the packet from the data bus;

receiving the frame check sequence of the copy of said packet and determining whether the packet contains an error, and producing an error detect signal and an error check result if said packet is determined as having an error;

storing in a register means the destination address, the source address and the data field of the copy of the packet, said error check result and the time-of-day data to produce an error record;

storing in a memory said error record in response to said error detect signal; and

reading stored error records from said memory.

FIG. 1

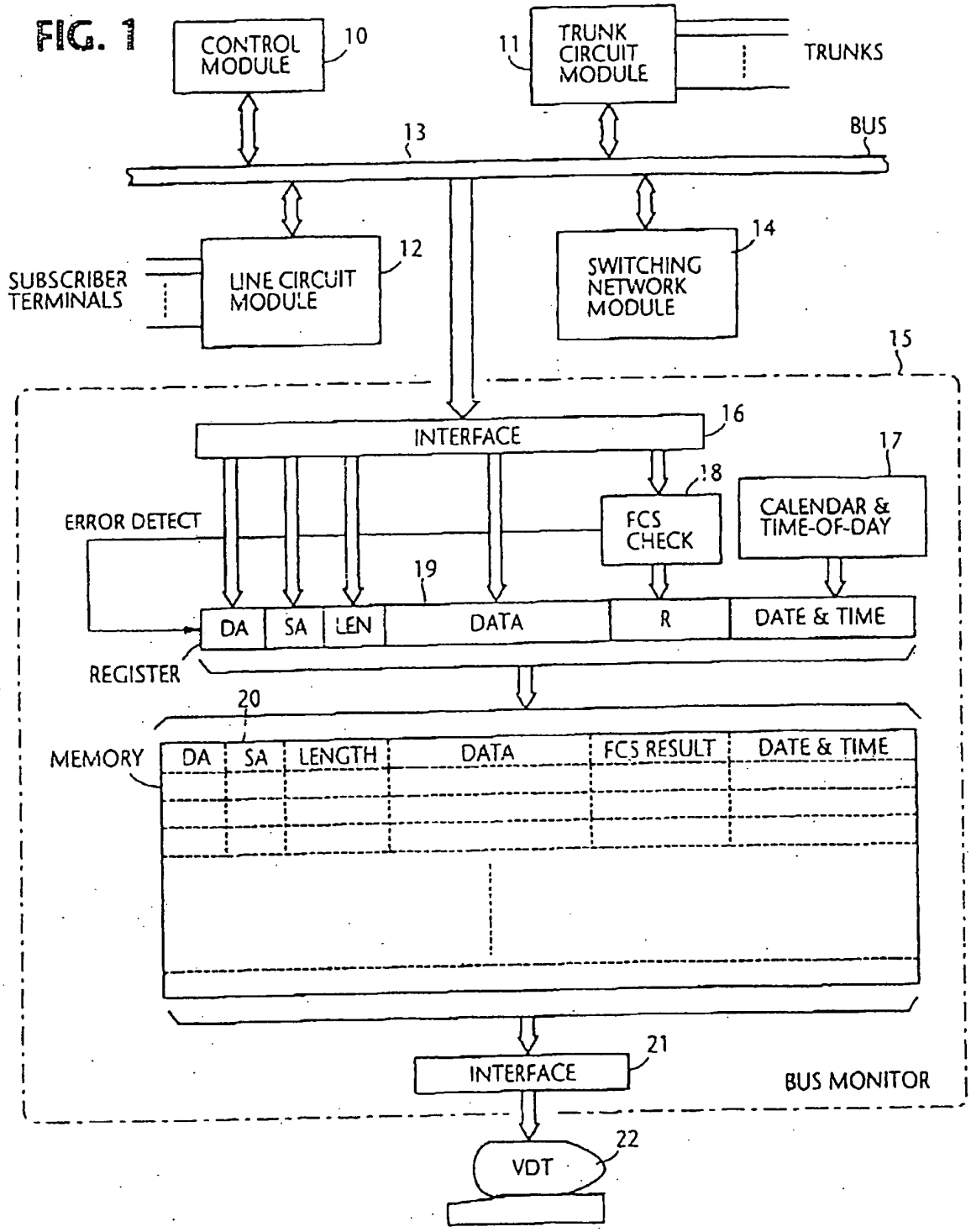
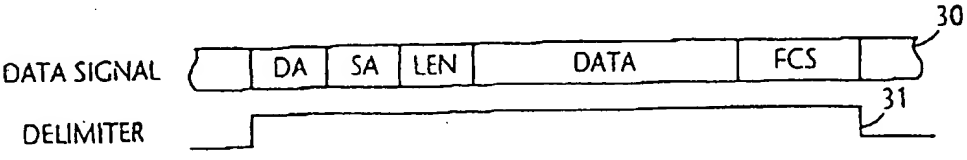

CONTROL MODULE
10
11
TRUNK CIRCUIT MODULE
TRUNKS
13
BUS
SUBSCRIBER TERMINALS
LINE CIRCUIT MODULE
12
SWITCHING NETWORK MODULE
14
15
INTERFACE
16
17
18
ERROR DETECT
FCS CHECK
CALENDAR & TIME-OF-DAY
19
DA
SA
LEN
DATA
R
DATE & TIME
REGISTER
20
MEMORY
DA
SA
LENGTH
DATA
FCS RESULT
DATE & TIME
INTERFACE
21
BUS MONITOR
VDT
22

FIG. 2


DATA SIGNAL
DA
SA
LEN
DATA
FCS
30
DELIMITER
31

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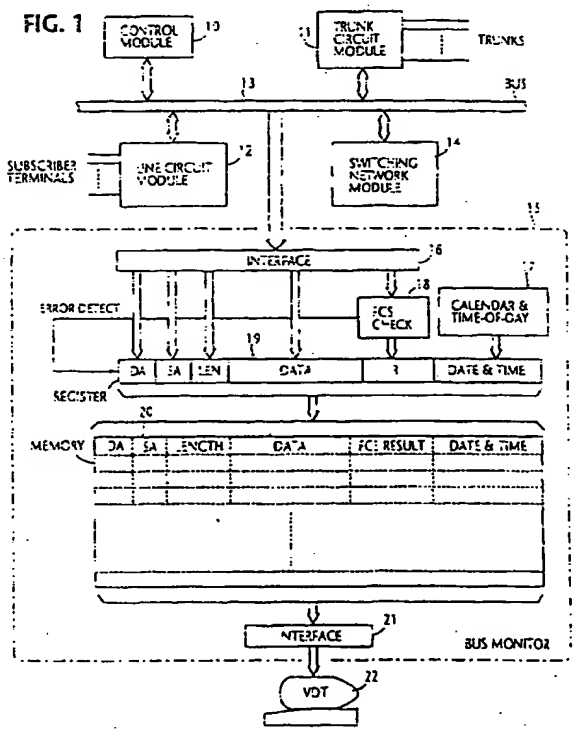

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EUROPEAN SEARCH REPORT

Application Number
EP 93 30 9545

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
Y	IBM TECHNICAL DISCLOSURE BULLETIN, vol.34, no.2, July 1991, NEW YORK US pages 98 - 99, XP210584 'HIGH-SPEED NETWORK ADAPTER ERROR TRACE MECHANISM' * the whole document * ---	1-6	H04L12/26
Y	HEWLETT-PACKARD JOURNAL, vol.43, no.5, October 1992, PALO ALTO US pages 34 - 40, XP349772 R.J.PRUFER 'NETWORK ADVISOR PROTOCOL ANALYSIS: DECODES' * figure 1 * * figure 2 * * figure 3 * -----	1-6	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	5 July 1995	Canosa Areste, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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